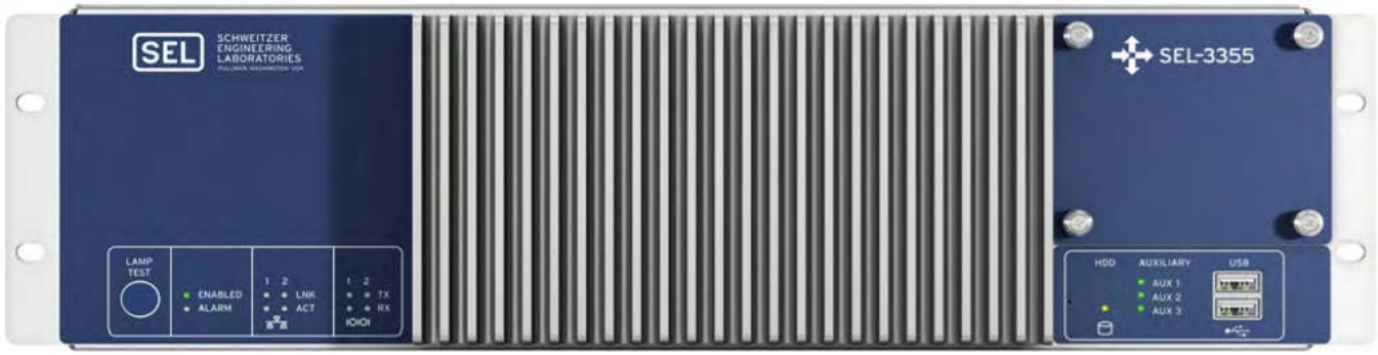
EXHIBIT B

US6603330	SEL-3355 Automation Controller ("The Accused Product")
25. A method of programming a programmable digital circuit block, comprising the steps of:	The accused product discloses a method of programming a programmable digital circuit block (e.g., DDR 3 SDRAM). SEL-3355 Automation Controller Improve Reliability, Availability, and Serviceability With a Rugged Automation Controller  The SEL-3355 Automation Controller uses a high-performance x86-64 architecture processor to support modern operating systems like Microsoft Windows and Linux. The extremely rugged SEL hardware of the SEL-3355 enables you to use your choice of automation controller operating system and software in very harsh environments not suitable for general purpose computers. https://cdn.selinc.com/assets/Literature/Product%20Literature/Data%20Sheets/3355_DS_20201210.pdf?v=20201231-181902

General

Supported Operating Systems

Microsoft Windows 7
Microsoft Windows 8/8.1
Microsoft Windows 10*
Microsoft Windows Server 2008 R2
Microsoft Windows Server 2012 R2
Microsoft Windows Server 2016*
CentOS Linux 6
CentOS Linux 7
Red Hat Enterprise Linux 6
Red Hat Enterprise Linux 7
VMware ESXi (Contact SEL for hardware and version compatibility)
* Orderable as a factory-installed option.

CPU

Intel Core i7-3555LE Dual-Core

Speed:	2.5 GHz base, 3.2 GHz turbo
Cache:	2 x 256 KB L2, 4 MB L3

Intel Core i7-3612QE Quad-Core

Speed:	2.1 GHz base, 3.1 GHz turbo
Cache:	4 x 256 KB L2, 6 MB L3

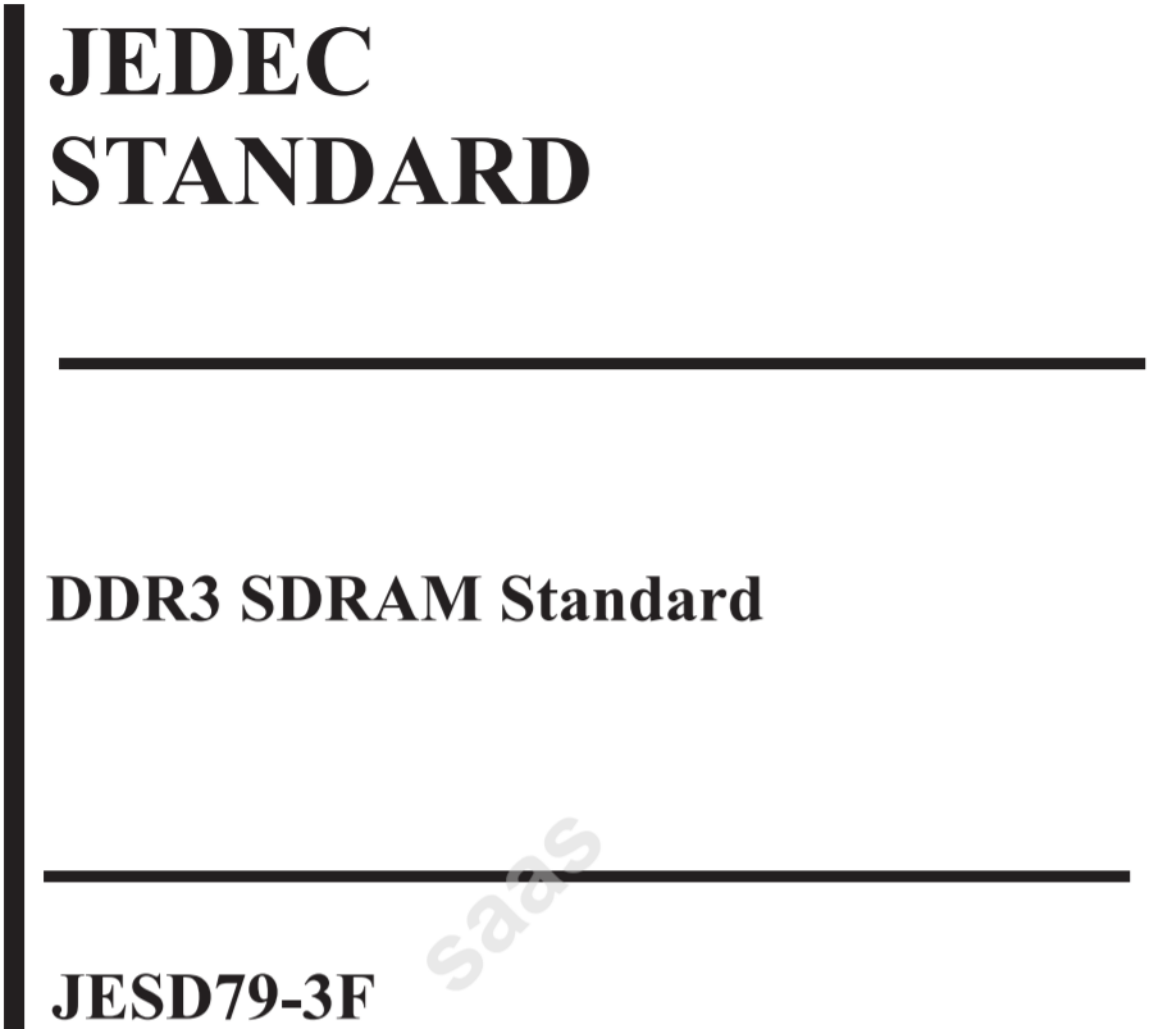
RAM

4–16 GB DDR3 ECC PC3-10600 (1333 MHz)

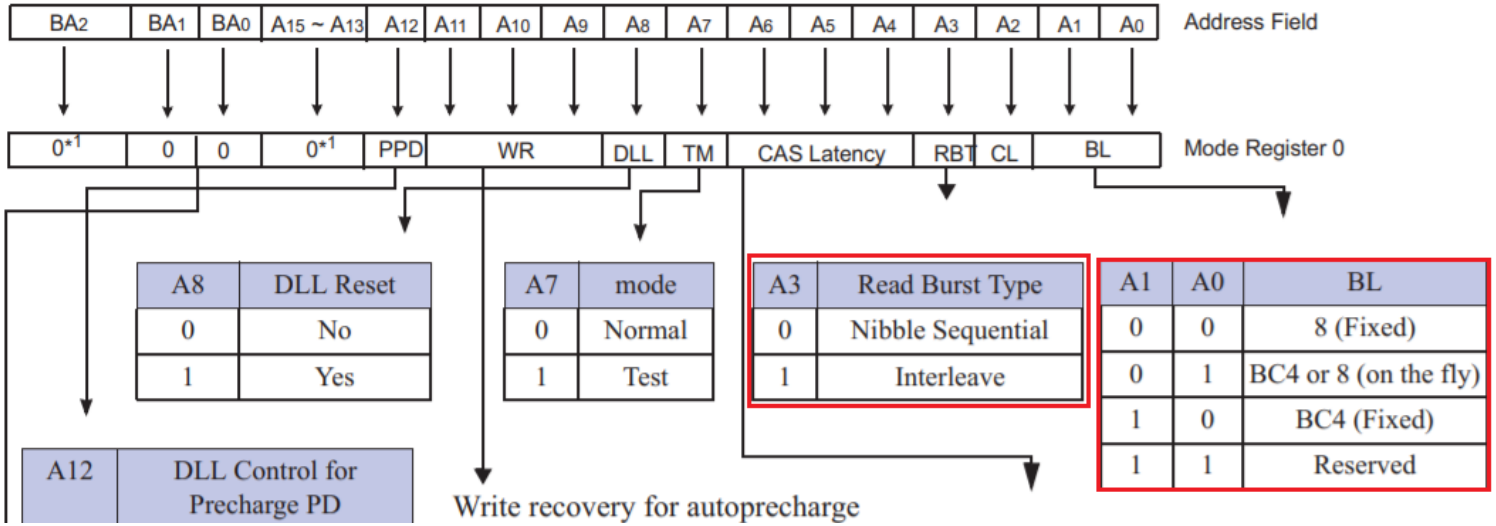
Chipset

Intel QM77 Express Chipset

https://cdn.selinc.com/assets/Literature/Product%20Literature/Data%20Sheets/3355_DS_20201210.pdf?v=20201231-181902

	 Source: DDR 3 standard
a) loading a plurality of	The accused product discloses loading a plurality of configuration data (e.g., bits A1, A0) corresponding to any one of

configuration data corresponding to any one of a plurality of predetermined digital functions into a configuration register of said programmable digital circuit block; and	a plurality of predetermined digital functions (e.g., read/write operations of fixed burst length of BC8 or BC4; read/write operations of on-the-fly burst length of BC8 or BC4) into a configuration register (e.g., Mode register MR0) of said programmable digital circuit block (e.g., DDR 3 SDRAM). **3.4.1 Programming the Mode Registers** For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. Source: DDR 3 standard **3.4.2 Mode Register MR0** The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, Source: DDR 3 standard

<table>
<tr><td></td><td>
3.4 Register Definition (Cont'd)
<u>3.4.2 Mode Register MR0</u> (Cont'd)
while controlling the states of address pins according to Figure 9.


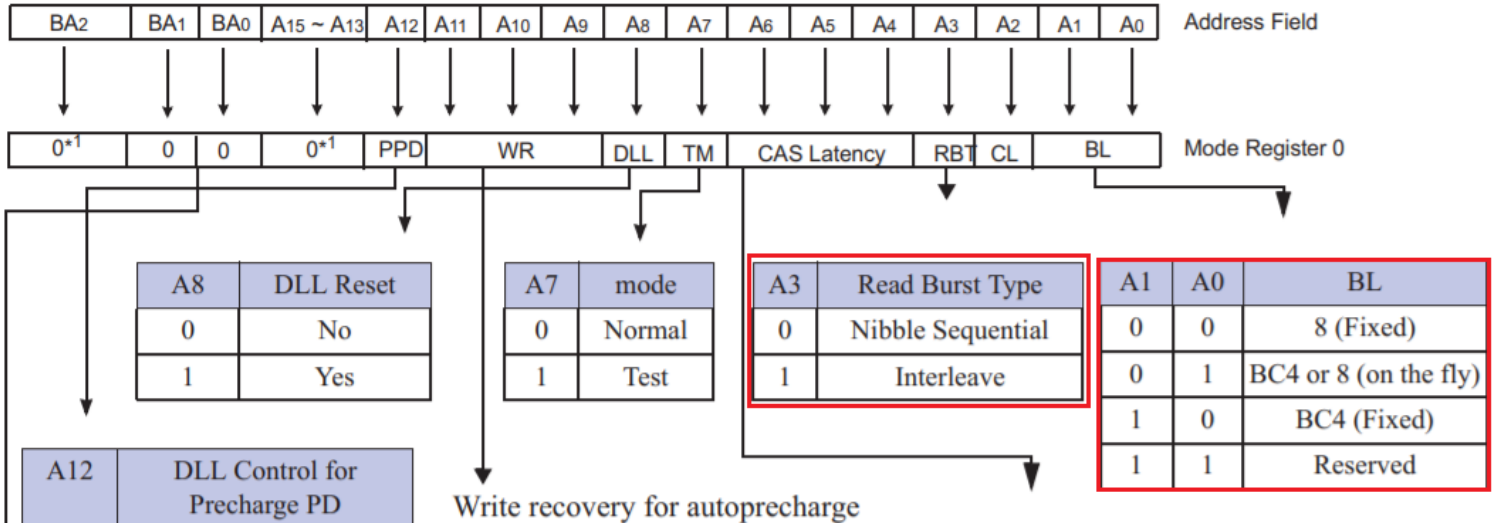
Source: DDR 3 standard
</td></tr>
<tr><td>b) configuring said programmable digital circuit block to perform any one of said plurality of predetermined digital functions based on said configuration data, wherein said steps a) and b) are dynamically</td><td>The accused product discloses configuring said programmable digital circuit block (e.g., DDR 3 SDRAM) to perform any one of said plurality of predetermined digital functions (e.g., read/write operations of fixed burst length of BC8 or BC4; read/write operations of on-the-fly burst length of BC8 or BC4) based on said configuration data (e.g., bits A1, A0), wherein said steps a) and b) are dynamically performed (e.g., on-the-fly BC is dynamically performed based on MRS command), and wherein said programmable digital circuit block includes a data register (e.g., register storing) for storing data to facilitate performing any one of said plurality of predetermined digital functions.

The data is bit A12. It is used according to the configuration data MR0 [A1, A0] to facilitate performing any one of the predetermined digital functions. For instance, if MR0[A1, A0] indicates on-the-fly (OTF) burst length, then A12 determines if the OTF burst length is BC4 or 8, and hence facilitates performing the read/write operations of OTF</td></tr>
</table>

performed, and wherein said programmable digital circuit block includes a data register for storing data to facilitate performing any one of said plurality of predetermined digital functions.	burst length BC4 or 8. **3.4.1 Programming the Mode Registers** For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. Source: DDR 3 standard **3.4.2 Mode Register MR0** The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, Source: DDR 3 standard

3.4 Register Definition (Cont'd)
3.4.2 Mode Register MR0 (Cont'd)

while controlling the states of address pins according to Figure 9.



Source: DDR 3 standard

Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

Source: DDR 3 standard

A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

Source: DDR 3 standard